Claims:

1. An injection-locked demodulator circuit with Automatic Frequency Control (AFC) that can be disabled.

2. The injection-locked demodulator circuit of claim 1, further comprising:

an injection-locked oscillator having a first input for receiving a modulated signal;

a multiplier having a first input for receiving the modulated signal and a second input for receiving a signal generated by the injection-locked oscillator;

a tuning circuit coupled to an output of the multiplier for receiving first and second input signals; and

a filter having an input coupled to an output of the tuning circuit and an output coupled to a second input of the injection-locked oscillator.

3. The injection-locked demodulator circuit of claim 2, wherein the AFC is disabled until a difference in first and second input signals reaches a threshold value.

4. The injection-locked demodulator circuit of claim 2, wherein the tuning circuit further includes:

first and second current mirrors coupled between a first input terminal that receives the first input signal and the output of the tuning circuit, the first current mirror receiving a first current and the second current mirror providing a first portion of an output current;

third, fourth and fifth current mirrors coupled between a second input terminal that receives the second input signal and the output terminal of the tuning circuit, the third current mirror receiving the second current and the fifth current mirror providing a second portion of the output current, wherein the first and second input terminals receive a differential signal from the multiplier; and

first and second transistors coupled from inputs of the respective second and fourth current mirrors to a first power supply conductor for preventing the second current mirror from providing the first portion of the output current and the fifth current mirror from providing the second portion of the output current.

5. The injection-locked demodulator circuit of claim 4, wherein the first current mirror comprises first and second P-channel MOS transistors having source terminals commonly coupled to a second power supply conductor and gate terminals commonly coupled to a drain terminal of the first P-channel MOS transistor and to the first input terminal.

6. The injection-locked demodulator circuit of claim 5, wherein the second current mirror comprises first and second NPN transistors having emitter terminals commonly coupled to the first power supply conductor and base terminals commonly coupled to a collector terminal of the first NPN transistor and to a drain terminal of the second P-channel MOS transistor.

7. The injection-locked demodulator circuit of claim 4, wherein the third current mirror comprises first and second P-channel MOS transistors having source terminals commonly coupled to a second power supply conductor and gate terminals commonly coupled to a drain terminal of the first P-channel transistor and to the second input terminal.

8. The injection-locked demodulator circuit of claim 7, wherein the fourth current mirror comprises first and second NPN transistors (32 and 34) having emitter terminals commonly coupled to the first power supply conductor (GND) and base terminals commonly coupled to a collector of the second NPN transistor (34) and to a drain of the second P-channel MOS transistor (36).

9. The injection-locked demodulator circuit of claim 8, wherein the fifth current mirror comprises third and fourth P-channel MOS transistors (28 and 30) having source terminals commonly coupled to the second power supply conductor and gate terminals commonly coupled to a drain of the fourth P-channel MOS transistor and to a collector terminal of the first NPN transistor.

10. The injection-locked demodulator circuit of claim 2, wherein the AFC is enabled when the modulated signal has no data and disabled when the modulated signal has data.

11. The injection-locked demodulator circuit of claim 10, wherein the tuning circuit further includes another input for receiving a signal that controls when the AFC is enabled and disabled.

12. The injection-locked demodulator circuit of claim 11, wherein the tuning circuit further includes:

first and second current mirrors coupled between a first input terminal that receives the first input signal and the output terminal of the tuning circuit, the first current mirror receiving a first current and the second current mirror providing a first portion of the output current; and

third, fourth and fifth current mirrors coupled between a second input terminal that receives the second input signal and the output terminal of the tuning circuit, the third current mirror receiving the second current and the fifth current mirror providing a second portion of the output current, wherein the first and second input terminals receive the differential signal from the multiplier.

13. The injection-locked demodulator circuit of claim 12, wherein the tuning circuit further includes:

a first switch coupled from an input of the second current mirror to a first power

supply conductor and preventing the second current mirror from providing the first portion of the output current; and

a second switch coupled from an input of the fourth current mirror to the first power supply conductor and preventing the fifth current mirror from providing the second portion of the output current at the output of the tuning circuit.

14. The injection-locked demodulator circuit of claim 13, wherein conduction of the first and second switches is controlled by the signal received at the another input of the tuning circuit.

15. A circuit for providing an automatic frequency control signal having first and second input terminals coupled for receiving a differential current and an output terminal that supplies a current that is a function of a difference of the differential current, the circuit comprising:

a first current path from the first input terminal to the output terminal;

a second current path from the second input terminal to the output terminal; and

first and second switches coupled for receiving a signal that disables the respective first and second current paths from providing the current that is the function of the difference of the differential current.

16. The circuit of claim 15, wherein the first current path includes first and second current mirrors coupled between the first input terminal and the output terminal of the circuit, the first current mirror receiving the first current and the second current mirror providing a first portion of the output current.

17. The circuit of claim 16, wherein the second current path includes third, fourth and fifth current mirrors coupled between the second input terminal and the output terminal of the circuit, the third current mirror receiving the second current and

the fifth current mirror providing a second portion of the output current.

18. The circuit of claim 17, wherein the first and second switches are coupled from the respective second and fourth current mirrors to a first power supply conductor and prevent the second current mirror from providing the first portion of the output current and the fifth current mirror from providing the second portion of the output current that combine at the output terminal of the circuit to provide the function of the difference in the first and second currents.

19. A tuning circuit having first and second input terminals and generating an automated frequency control signal at an output terminal, comprising:

first and second transistors that form a first current mirror and have first current conduction terminals commonly coupled to a first power supply conductor and control terminals commonly coupled to a second current conduction terminal of the first transistor and to the first input terminal;

third and fourth transistors that form a second current mirror and have first current conduction terminals commonly coupled to a second power supply conductor and control terminals commonly coupled to a second conduction terminal of the third transistor and to a second current conduction terminal of the second transistor;

fifth and sixth transistors that form a third current mirror and have first current conduction terminals commonly coupled to the first power supply conductor and control terminals commonly coupled to a second current conduction terminal of the sixth transistor and to the second input terminal;

seventh and eighth transistors that form a fourth current mirror and have first current conduction terminals commonly coupled to the second power supply conductor and control terminals commonly coupled to a second conduction terminal of the eighth transistor and to a second conduction terminal of the fifth transistor; and

ninth and tenth transistors that form a fifth current mirror and have first current conduction terminals commonly coupled to the first power supply conductor and

control terminals commonly coupled to a second conduction terminal of the tenth transistor and to a second conduction terminal of the seventh transistor, and the second conduction terminal of the ninth transistor being coupled to the output terminal of the tuning circuit.

20. The circuit of claim 19, further including:

an eleventh transistor having a control terminal coupled to the first input terminal and a first conduction terminal coupled to the first power conductor; and

a twelfth transistor having a control terminal and a first conduction terminal coupled to a second conduction terminal of the eleventh transistor and an second conduction terminal coupled to the second power conductor.

21. The circuit of claim 20, further including:

an thirteenth transistor having a control terminal coupled to the second input terminal and a first conduction terminal coupled to a first power conductor; and

a fourteenth transistor having a control terminal and a first conduction terminal coupled to a second conduction terminal of the thirteenth transistor and a second conduction terminal coupled to the second power conductor.

22. The circuit of claim 21, further including:

a fifteenth transistor having a control terminal coupled to the control terminal of the fourteenth transistor, a first conduction terminal coupled to the second power conductor and a second conduction terminal coupled to the second conduction terminal of the second transistor; and

a sixteenth transistor having a control terminal coupled to a control terminal of the twelfth transistor, a first conduction terminal coupled to the second power conductor and a second conduction terminal coupled to the second conduction terminal of the fifth transistor.

23. The circuit of claim 22, wherein scaling provides a current gain in a current signal path through the sixth, thirteenth, fourteenth and fifteenth transistors that exceeds a current gain in a current signal path through the first and second transistors, and a current gain in a current signal path through the first, eleventh, twelfth and sixteenth transistors exceeds a current signal path through the sixth and fifth transistors.

24. A method for generating an Automatic Frequency Control (AFC) signal having a dead band region where the AFC signal is not responsive to a difference in first and second input signals, comprising:

transferring a first signal received at a first input to an output through a first path;

transferring a second signal received at a second input to the output through a second path for combining with the first signal in generating the AFC signal; and

exceeding a threshold in the AFC before generating the dead band region by transferring the first and second signals to the output.

25. A method for generating an Automatic Frequency Control (AFC) signal based on a modulated signal, comprising:

enabling a tuning circuit for generating the AFC signal as a function of a difference in first and second currents supplied to the tuning circuit when data is not present in the modulated signal; and

disabling the AFC signal when data is present in the modulated signal.

26. A method for generating an Automatic Frequency Control (AFC) signal in an injection-locked demodulator, comprising:

providing the injection-locked demodulator with an unmodulated signal at the carrier frequency of the modulated signal;

providing the injection-locked demodulator with a modulated signal; and

disabling the AFC signal in the presence of the modulated signal to prevent detuning the injection-locked demodulator.

27. A method of generating an Automatic Frequency Control (AFC) signal in an injection-locked demodulator, comprising:

tuning the injection-locked demodulator when a threshold value is exceeded; and

allowing only that portion of the AFC signal that exceeds the threshold value to pass to an AFC filter and an oscillator.